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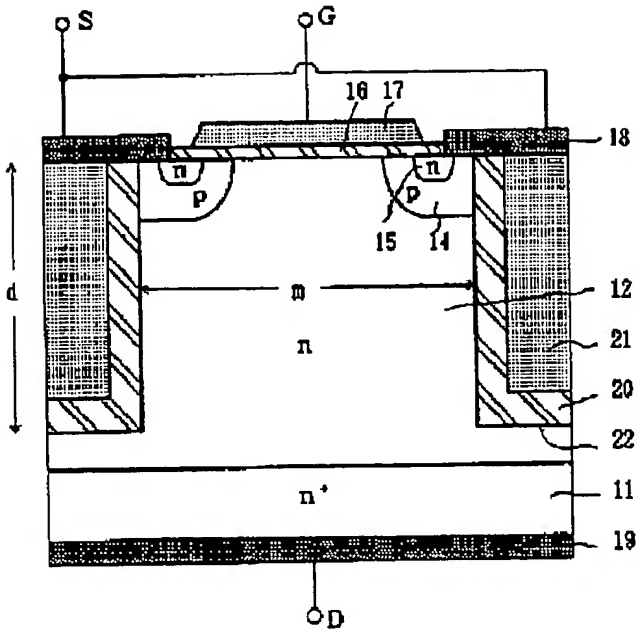
TITLE : VERTICAL MOSFET



ABSTRACT : PROBLEM TO BE SOLVED: To provide a vertical MOSFET, the on-resistance of which can be lowered and which can be manufactured easily.

SOLUTION: A vertical MOSFET has p-type well regions 14 formed in the surface layer of an n-type drift area 12 on an n+-type drain layer 11, n-type source regions 15 in the well regions 14, and a gate electrode 17 provided on the surfaces of the well regions 14 sandwiched between the source regions 15 and drift region 12 via a gate insulating film 16. The MOSFET also has source electrodes 18, which are commonly brought into contact with the source regions 15 and well regions 14. In the MOSFET, the impurity concentration distribution in the drift region 12 is adjusted, so that the concentration becomes gradually linearly higher with the depth. In addition, trenches 22 are dug in the MOSFET from the surfaces of the well regions 14, and polycrystalline silicon 21 which is short-circuited to the source electrodes 18 is buried in the trenches 22 through thick insulating films 20.

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(54) (Title of the invention) Vertical MOSFET

(57) (Abstract)
(Problem) To provide a vertical MOSFET which allows the ON resistance to be markedly lowered and which is easy to manufacture.
(Solution) In a vertical MOSFET having a p well layer 14 formed in the top surface layer of an n drift region 12 located over an n^+ drain layer 11; an n source region 15 formed inside the p well region 14; a gate electrode 17 provided across a gate insulation film 16 on the top surface of the p well region 14 between the n source region 15 and n drift region 12; and provided with a source electrode 18 that has a common contact with the top surface of the p well region 14 and n source region 15, the dopant concentration distribution of the n drift region 12 is made into a linear distribution whereby the concentration becomes higher in the depth direction, a trench 22 is dug down from the top surface of the p well region 14, and polycrystalline silicon 21 shorted to the source electrode is buried inside the trench 22 across a thick insulation film 20.

[see source for figure]

11	n^+ drain layer	18	source electrode
12	n drift region	19	drain electrode
14	p well region	20	trench insulation film
15	n source region	21	polycrystalline silicon
16	gate insulation film	22	trench
17	gate electrode		

(Scope of patent claims)

(Claim 1) A vertical MOSFET containing a low concentration drift region of a first conductivity type formed over a high concentration substrate of a first conductivity type; a well region of a second conductivity type formed selectively in the top surface layer of said drift region; a source region of the first conductivity type formed inside said well region of the second conductivity type; a gate electrode provided across an insulation film on the top surface of the well region of the second conductivity type between the drift region of the first conductivity type and the source region of the first conductivity type; a source electrode having common contact with the top surface of the well region of the second conductivity type and the source region of the first conductivity type; and a drain electrode provided on the bottom surface of the substrate of the first conductivity type, said vertical MOSFET being distinguished in that it contains a trench which is dug down from the top surface of the well region of the second conductivity type and extends to the vicinity of the substrate of the first conductivity type, and a conductor provided along the inner wall of the trench over a thick insulating film that can withstand the element withstand voltage, said conductor being shorted to the source electrode.

(Claim 2) A vertical MOSFET as set forth in Claim 1, distinguished in that the drift region of the first conductivity type has a linear concentration gradient whereby the concentration becomes higher in the depth direction.

(Claim 3) A vertical MOSFET as set forth in Claim 2, distinguished in that the drift region of the first conductivity type has a concentration gradient of the following formula in the depth direction (y).

(Formula 1)

[see source for formula]

wherein ε_s is the dielectric constant of the semiconductor, ε_{ox} is the dielectric constant of the oxide film, q is the elementary charge, m is the width of the mesa part of the trench, t_{ox} is the oxide film thickness, BV is the withstand voltage and d is the depth of the trench.

(Claim 4) A vertical MOSFET as set forth in any of Claims 1 through 3, distinguished in that the semiconductor is silicon.

(Claim 5) a vertical MOSFET as set forth in any of Claims 1 through 3, distinguished in that the semiconductor is silicon carbide.

(Detailed description of the invention)

(0001)

(Technical field of the invention) The present invention relates to the structure of electric power MOSFETs employing high resist voltage semiconductor elements, especially MOSFETs.

(0002)

(Prior art) Heretofore, the characteristics of vertical power MOSFETs were restricted by the tradeoff relationship between the withstand voltage and the ON resistance. It is known that in a power MOSFET having the optimal structure, the ON resistance R_{DSon} has the following relationship to the withstand voltage BV:

$R_{DSon} \propto BV^{2.4-2.6}$. (1)

From this, it can be seen that as the withstand voltage is increased, the ON resistance will rise sharply.

(0003) However, in the withstand voltage class of 600 V or greater, the ON resistance of MOSFETs becomes too high, so low ON voltage insulated gate bipolar transistors (hereinafter referred to as IGBTs), which make use of the carrier multiplication effect, are frequently employed.

(0004) However, since IGBTs are bipolar elements, they have the problem of essentially poor switching characteristics, so again, the implementation of a low ON resistance MOSFET was still being anticipated.

(0005) Silicon carbide (hereinafter referred to as SiC) has extremely high maximum insulation strength compared to silicon, so in recent years, there has been active research and development on it aiming at power elements, with the expectation of being able to reduce the ON resistance by nearly three orders of magnitude. However, SiC has extremely different physical properties and process technology from silicon, so a new process technology needs to be developed, and this is still considered a future technology.

(0006) Recently, power MOSFETs of a new structure having a deep pn junction have been proposed (see G. Deboy, M. Maerz, J.-P. Stengl, H. Strack, J. Tihanyi and H. Weber, "A new generation of high voltage MOSFETs breaks the limit line of silicon", Technical Digest of IEDM98 (1998), p. 683). Figure 3 is a cross-sectional view of such a power MOSFET.

(0007) The part corresponding to the drift region of conventional vertical MOSFETs has been replaced with a parallel pn layer in which an n drift region 2 and p barrier region 3 are placed side by side in alternating fashion, with a p well region 4 being formed at one side of the parallel pn layer, and an n source region 5 being formed in the top surface layer thereof. An n^+ drain layer 1 is located at the other side of the parallel pn layer, and a drain electrode 9 is provided at the top surface of the n^+ drain layer 1. A gate electrode 7

is provided across a gate insulation film 6 on the top surface of the p well region 4 between the n drift region 2 and the source region 5. 8 is a source electrode, which is provided in common contact with the surface of the p well region 4 and n source region 5.

(0008) The intent of this structure is to maintain an ample withstand voltage even with a high concentration n drift region 2, by extending the depletion layer not just to the n drift region 2 but also to the p barrier region 3. Furthermore, by using this structure, it is possible to increase the concentration of the n drift region 2 in inverse proportion to its width: that is, the dopant concentration can be increased by reducing the width, thus making it possible raise the concentration of the n drift region 2 even in a high withstand voltage MOSFET, as a result allowing the ON resistance to be drastically lowered.

(0009)

(Problem to be solved by the invention) However, in a MOSFET with the structure of Figure 3, the thickness of the parallel pn layer consisting of the n drift region 2 and p barrier region 3 has to be increased to match the withstand voltage. Therefore, in order to implement this structure, each time 10 μm of the epitaxial film is deposited, it is necessary to perform diffusion of acceptor dopants to form the p barrier region 3.

(0010) For instance, in a 600 V element, epitaxial film and ion injection and heat treatment would need to be repeated about six times. This leads to a very large increase in the manufacturing process, accounting alone for about half of the entire manufacturing process. Namely, there is the problem that the manufacturing cost becomes nearly twice that of conventional elements. In view of this problem, the objective of the present invention is to provide a vertical MOSFET which allows the ON resistance to be markedly lowered and which is easy to manufacture.

(0011)

(Means of solving the problem) To solve the aforementioned problem, the present invention provides a vertical MOSFET comprising a low concentration drift region of a first conductivity type formed over a high concentration substrate of a first conductivity type; a well region of a second conductivity type formed selectively in the top surface layer of said drift region; a source region of the first conductivity type formed inside said well region of the second conductivity type; a gate electrode provided across an insulation film on the top surface of the well region of the second conductivity type between the drift region of the first conductivity type and the source region of the first conductivity type; a source electrode having common contact with the top surface of the well region of the second conductivity type and the source region of the first conductivity type; and a drain electrode provided on the bottom surface of the substrate of the first conductivity type, which vertical MOSFET is made to contain a trench which is dug down from the top surface of the well region of the second conductivity type and extends to the vicinity of the substrate of the first conductivity type, and a conductor provided along the inner wall of the trench over a thick insulating film that can withstand the element withstand voltage, said conductor being shorted to the source electrode.

(0012) By doing this, since the conductor provided along the inner wall of the trench is shorted to the source electrode, a depletion layer extends along the inner wall of the trench, making it possible to hold a withstand voltage. In particular, the drift region of the first conductivity type is made to have a specific concentration gradient in the depth direction, such as that of formula (2).

(0013)

(Formula 2)

[see source for formula]

Here, ε_s is the dielectric constant of the semiconductor, ε_{ox} is the dielectric constant of the oxide film, q is the elementary charge, m is the width of the mesa part of the trench, t_{ox} is the oxide film thickness, BV is the withstand voltage and d is the depth of the trench.

(0014) By doing this, the field strength inside the mesa part becomes uniform, making it possible to withstand high voltages. (S. Mahalingam and B. J. Baliga, "A Low Forward Drop High Voltage Trench MOS Barrier Schottky Rectifier with Linearly Graded Doping Profile", Proceedings of 1998 Int. Sym. Power Semiconductor Devices & ICs, Kyoto (1998), p. 187).

(0015) The semiconductor can be either silicon or silicon carbide; if it is silicon carbide, the field strength will be higher by about an order of magnitude, so the depth of the trench can be made about 1/10 of that in the case of silicon.

(0016)

(Modes of embodiment of the invention) (Embodiment example) Below, the present invention is described in detail while presenting embodiment examples. The silicon carbide described here, out of the many polymorphs that exist, as is well known, primarily refers to those known as 6H and 4H.

(0017) Figure 1 is a cross-sectional view of a vertical MOSFET that embodies the present invention. It will be described while comparing it to the cross-sectional view of the prior art in Figure 3. Over the n^+ drain region 11, there is an n drift region 12, on the top surface of which a p well region 14 is selectively formed, and an n source region 15 is formed inside the p well region 14, all this being the same as in the MOSFET of Figure 3. However, no p barrier region is provided, and instead, a trench 22 is dug down, and polycrystalline silicon 21 is embedded across an insulation film 20. A gate electrode 17 is provided across a gate insulation film 16 on the top surface of the p well region 14 between the n drift region 12 and n source region 15. A source electrode 18 is provided in common contact with the surface of the p well region 14 and n source region 15, and a drain electrode 19 is provided on the bottom surface of the n^+ drain layer 11. The source electrode 18 is also in contact with the polycrystalline silicon 21.

(0018) In the structure of the present invention in Figure 1, the junction area that maintains the withstand voltage is not a pn junction, but rather an MOS junction. The polycrystalline silicon 21 in which the trench 22 is embedded in Figure 1 is shorted by the p well region 14 and source electrode 18. Here, the n drift region 12 has a concentration distribution N(y) of the aforementioned formula (2) in the depth direction.

(0019) For example, in the case of a 1000 V withstand voltage class silicon MOSFET, the trench depth d is 60 μm, the mesa width m of the trench is 10 μm, the thickness t_{ox} of the oxide film 20 is 5 μm, the concentration near the top surface of the n drift region 12 is about 10^{15} cm^{-3}, and the concentration at the deepest location is 2×10^{16} cm^{-3}.

(0020) Figure 2 (a) through (c) is a cross-sectional drawing of a process sequence serving to explain the manufacturing process of the MOSFET of Figure 1. Here, the entire process is not illustrated, with only the basic parts being shown. Over the high concentration n type substrate, which becomes the n^+ drain layer 11, an n drift region 12 is grown by the epitaxial method (Figure 2 (a)). For maximum optimization, it is desirable to lower the concentration according to formula (2) as the growth progresses, but an overall effect of lowering the ON resistance will be obtained so long as the concentration is somewhat lower than the concentration given by formula (2).

(0021) After forming a pattern on the surface with a mask material such as, for example, SiO_2, etching is carried out to form a trench 22, of a depth that extends to the vicinity of the high concentration substrate (Figure 2 (b)). The trench 22 does not however necessarily have to extend to the high concentration substrate. For the etching, one can use plasma etching using CF_4 or the like, reactive etching, etc.

(0022) After forming an insulation film 20 on the inner wall of the trench 22 of the substrate by the CVD method, polycrystalline silicon 21 is embedded in the trench 22 (Figure 2 (c)). Here, the thickness of the insulation film 20 is important for maintaining the withstand voltage. That is, since the voltage between source and drain is directly impressed onto the oxide film, its withstand voltage needs to be maintained. For example, to obtain 100 V withstand voltage, a thickness of approximately 5 μm is needed. Subsequent processes are the same as in manufacturing conventional power MOSFETs, so description thereof will be omitted. In this way, the structure of Figure 1 can be manufactured.

(0023) In the case of a silicon MOSFET having an n drift region of uniform concentration, for 1000 V class, the dopant concentration of the n drift region is 2×10^{14} cm^{-3} (see D. A. Grand and J. Gowar, Power MOSFETs–Theory and Applications, John Wiley & Sons, Inc), while with the MOSFET of the present invention, the concentration is higher by 1 to 2 orders of magnitude, so the ON resistance is reduced to about 1/20.

(0024) Furthermore, the pn junction in Figure 3 consists of the n drift region 2 and p barrier region 3, and its thickness has to be increased to match the withstand voltage. For example, for 600 V, about 60 μm is necessary, and about 100 μm is needed for 1000 V. Moreover, to manufacturing this structure, assuming that epitaxial growth is repeated every 10 μm as discussed above, ten iterations of the process will be needed, greatly increasing the manufacturing costs. By using the structure of the present invention, it is possible to implement low ON resistance at high withstand voltage without employing an expensive manufacturing process that involves repeating epitaxial growth, ion injection and heat treatment processes.

(0025) (Embodiment example 2) In the case of SiC, for instance for 1000 V withstand voltage, the n drift region dopant concentration would be about 10^{16} cm^{-3} near the surface and 2×10^{17} cm^{-3} at the deepest place, making it possible to reduce the ON resistance in this case as well. In particular, in the case of SiC, the field strength is approximately one order of magnitude higher than for silicon, so the trench depth can be made 1/10 as deep compared to when using silicon, making this especially effective.

(0026)

(Effect of the invention) According to the present invention as described above, in a vertical MOSFET having a well region of a second conductivity type formed selectively in the top surface layer of a drift region of a first conductivity type having a linear dopant concentration distribution, whereby the concentration increases in the depth direction; a source region of the first conductivity type formed inside the well region; a gate electrode; a source electrode; and a drain electrode, a trench is dug down from top surface of the well region of the second conductivity type and a conductor, which is shorted to the source electrode, is provided inside the trench across a thick insulation film, thereby making it possible to implement a vertical MOSFET with high withstand voltage and low ON resistance. It suffices to provide the trench to a depth appropriate for the withstand voltage, and there is no increase in processes as was the case with the conventional structure. Therefore, the number of manufacturing processes is low and the MOSFET can be manufactured inexpensively.

(Brief description of the drawings)

(Figure 1) A cross-sectional view of a vertical MOSFET according to the present invention.

(Figure 2) (a) through (c) is a cross-sectional view of the manufacturing process sequence for the MOSFET of Figure 1.

(Figure 3) Cross-sectional view of a conventional vertical MOSFET

(Description of captions)

1, 11 n^+ drain layer
2, 12 n drift region
3 p barrier region
4, 14 p well region
5, 15 n source region
6, 16 gate insulation film
7, 17 gate electrode
8, 18 source electrode
9, 19 drain electrode
10, 20 insulation film
21 polycrystalline silicon
22 trench
23 mask material

(Figure 1)

[see source for figure]

(Figure 2)

[see source for figure]

11 n^+ drain layer
12 n drift region
14 p well region
15 n source region
16 gate insulation film
17 gate electrode
18 source electrode
19 drain electrode
20 trench insulation film
21 polycrystalline silicon
22 trench

(Figure 3)

[see source for figure]

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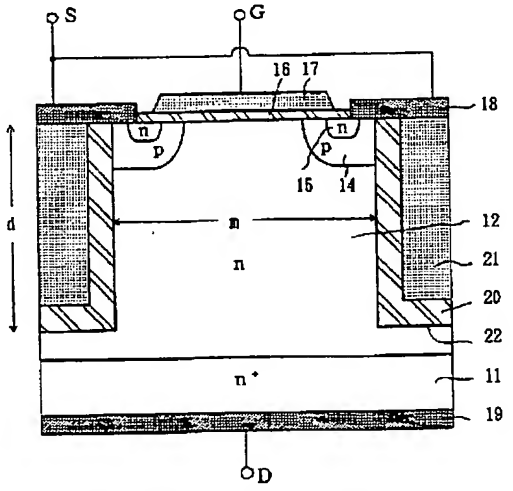
(54)【発明の名称】　縦型ＭＯＳＦＥＴ

(57)【要約】
【課題】オン抵抗を著しく下げることが可能でしかも製造の容易な縦型ＭＯＳＦＥＴを提供する。
【解決手段】n^+ ドレイン層１１上のｎドリフト領域１２の表面層にｐウェル領域１４が形成され、そのｐウェル領域１４内にｎソース領域１５が形成され、ｎソース領域１５とｎドリフト領域１２とに挟まれたｐウェル領域１４の表面上にゲート絶縁膜１６を介してゲート電極１７が設けられ、ｎソース領域１５とｐウェル領域１４との表面に共通に接触するソース電極１８が設けられた縦型ＭＯＳＦＥＴにおいて、ｎドリフト領域１２の不純物濃度分布を深さ方向に次第に高くなる直線的な分布とし、ｐウェル領域１４の表面からトレンチ２２を掘り下げ、そのトレンチ２２内に厚い絶縁膜２０を介してソース電極と短絡される多結晶シリコン２１を埋める。



11 n^+ ドレイン層	18 ソース電極
12 ｎドリフト領域	19 ドレイン電極
14 ｐウェル領域	20 トレンチ絶縁膜
15 ｎソース領域	21 多結晶シリコン
16 ゲート絶縁膜	22 トレンチ

ト領域2とnソース領域5とに挟まれたpウェル領域4の表面上にはゲート絶縁膜6を介してゲート電極7が設けられている。Sはソース電極であり、nソース領域5とpウェル領域4の表面に共通に接触して設けられている。

【0008】この構造の意図は、nドリフト領域2だけではなく、p仕切り領域3にも空乏層を広げることによって、高い濃度のnドリフト領域2でも充分に耐圧を維持しようとするものである。そして、この構造を用いるとnドリフト領域2の濃度をその幅に逆比例して増加させることが可能であり、すなわち幅を狭くすれば不純物濃度を高くすることができるので、高耐圧MOSFETでもnドリフト領域2の濃度を高めに設定でき、結果としてオン抵抗を著しく下げることが可能である。

【0009】

【発明が解決しようとする課題】しかし、図3の構造のMOSFETは、nドリフト領域2とp仕切り領域3とからなる並列pn層の厚さを耐圧に合わせて大きくしなければならない。従って、この構造を実現するためには、エピタキシャル膜を10μm程度積むたびに、p仕切り領域3を形成するためのアクセプタ不純物の拡散を行っていく必要がある。

【0010】例えば600V素子ではエピタキシャル膜とイオン注入、および熱処理を6回程度繰り返すことになる。これは非常に大きな製造工程の増加につながり、それだけで全体の製造工程のほぼ半分を占めることになる。すなわち従来の素子と比較して製造コストが2倍近くになるという問題がある。このような問題に鑑み本発明の目的は、オン抵抗を著しく下げることが可能でしかも製造の容易な縦型MOSFETを提供することにある。

【0011】

【課題を解決するための手段】上記課題解決のため本発明は、高濃度の第一導電型基板上に形成された低濃度の第一導電型ドリフト領域と、その表面層に選択的に形成された第二導電型ウェル領域と、その第二導電型ウェル領域内に形成された第一導電型ソース領域と、第一導電型ドリフト領域と第一導電型ソース領域とに挟まれた第二導電型ウェル領域の表面上に絶縁膜を介して設けられたゲート電極と、第一導電型ソース領域と第二導電型ウェル領域との表面に共通に接触するソース電極と、第一導電型基板の裏面に設けられたドレイン電極とを有する縦型MOSFETにおいて、第二導電型ウェル領域の表面から掘り下げられた第一導電型基板近くに達するトレンチと、そのトレンチ内壁に沿って素子耐圧に耐える厚い絶縁膜を介して設けられた導電体とを備え、その導電体がソース電極と短絡されているものとする。

【0012】そのようにすれば、トレンチ内壁に沿って設けられた導電体がソース電極と短絡されているので、トレンチ内壁に沿って空乏層が広がり、耐圧を保持することができる。特に、第一導電型ドリフト領域が深さ方向に、例えば式(2)のような所定の濃度勾配をもつものとする。

【0013】

【数2】

$$N(y)=\left[\frac{\varepsilon_s}{\frac{qm}{2}\left[\frac{\varepsilon_s}{\varepsilon_{ox}}t_{ox}+\frac{m}{4}\right]}\right]\left[\frac{BV}{d-t_{ox}}\right]y \quad (2)$$

ここで

ε_s：半導体の誘電率、ε_{ox}：酸化膜の誘電率、q：素電荷、m：トレンチのメサの部分の幅、t_{ox}：酸化膜厚、BV：耐圧、d：トレンチの深さである。

【0014】そのようにすれば、メサ内部の電界強度が均一化され、、高電圧に耐えるようにすることができる〔S.Mahalingam and B.J.Baliga "A Low Forward Drop HighVoltage Trench MOS Barrier Schottky Rectifier with Linearly Graded Doping Profile", Proceedings of 1998 Int. Sym. Power Semiconductor Devices & IC s, Kyoto (1998), p.187〕。

【0015】半導体は、シリコンであっても、炭化珪素であってもよく、炭化珪素であれば、電界強度が約一桁大きいので、トレンチの深さをシリコンの場合の略1／10にできる。

【0016】

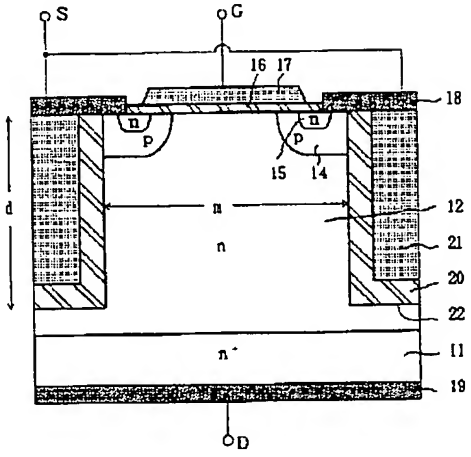
【発明の実施の形態】〔実施例〕以下で本発明について、実施例を示しながら詳細に説明する。なお、ここで説明する炭化珪素は良く知られているように、存在する多くの多形の内、主に6Hおよび4Hと呼ばれるものを

【図3】従来の縦型ＭＯＳＦＥＴの断面図

【符号の説明】

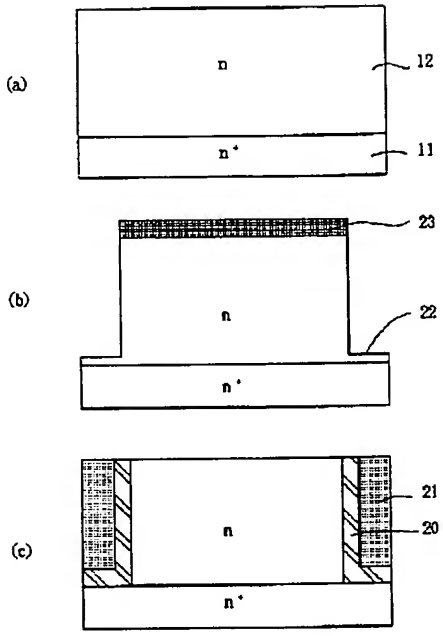
1、11　n⁺ ドレイン層
2、12　nドリフト領域
3　p仕切り領域
4、14　pウェル領域
5、15　nソース領域
6、16　ゲート絶縁膜
7、17　ゲート電極
8、18　ソース電極
9、19　ドレイン電極
10、20　絶縁膜
21　多結晶シリコン層
22　トレンチ
23　マスク材

【図1】



11 n⁺ ドレイン層
12 nドリフト領域
14 pウェル領域
15 nソース領域
16 ゲート絶縁膜
17 ゲート電極
18 ソース電極
19 ドレイン電極
20 トレンチ絶縁膜
21 多結晶シリコン
22 トレンチ

【図2】



【図3】